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<b>(51) International Patent Classification 7 :</b>  <b>G06F 13/00</b>	<b>A2</b>	<b>(11) International Publication Number:</b> <b>WO 00/17759</b>  <b>(43) International Publication Date:</b> 30 March 2000 (30.03.00)
<b>(21) International Application Number:</b> PCT/GB99/03089  <b>(22) International Filing Date:</b> 16 September 1999 (16.09.99)  <b>(30) Priority Data:</b> 9820430.8 18 September 1998 (18.09.98) GB 9820428.2 18 September 1998 (18.09.98) GB 9820412.6 18 September 1998 (18.09.98) GB 9820410.0 18 September 1998 (18.09.98) GB  <b>(71) Applicant (for all designated States except US):</b> PIXELFUSION LIMITED [GB/GB]; 2440 The Quadrant, Aztec West, Almondsbury, Bristol BS32 4AQ (GB).  <b>(72) Inventors; and</b> <b>(75) Inventors/Applicants (for US only):</b> PHELPS, Richard, Carl [GB/GB]; 13 Oxbarton, Stoke Gifford, Bristol BS34 8RP (GB). WINSER, Paul, Anthony [GB/GB]; 32 Epsom Close, Downend, Bristol BS16 6ST (GB).  <b>(74) Agent:</b> HASELTINE LAKE & CO.; Imperial House, 15-19 Kingsway, London WC2B 6UD (GB).		<b>(81) Designated States:</b> AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).  <b>Published</b> <i>Without international search report and to be republished upon receipt of that report.</i>
<b>(54) Title:</b> APPARATUS FOR USE IN A COMPUTER SYSTEM  <b>(57) Abstract</b>  Apparatus for use in a computer system comprises a bus architecture, a plurality of modules connected to the bus architecture, at least one module being latency tolerant and at least one module being latency intolerant. The bus architecture comprises a primary bus (3) having latency intolerant modules connected thereto, a secondary bus (4) having latency tolerant modules connected thereto, and a primary to secondary bus interface module (5) interconnecting the primary and secondary buses.		

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